IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Rhee et al.**	§
	§ Group Art Unit: **Not Assigned**
Serial No.: **Not Assigned**	§
	§ Examiner: **Not Assigned**
Filed: **October 29, 2003**	§
	§ Attorney Docket No.: **YOR920030387US1**
For: **Semidigital Delay-Locked Loop Using an Analog-Based Finite State Machine**	§

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request that the information listed on the attached Form PTO-1449 be considered by the Office during the pendency of the above entitled application, pursuant to 37 C.F.R. 1.97.

Please charge any fees necessary for prosecution of the present application to Deposit Account No. 50-0510. If any extension of time is required, such extension is hereby requested. Please charge any additional required fee for extension of time to Deposit Account No. 50-0510.

In accordance with 37 C.F.R. 1.97(h), the filing of this Information Disclosure Statement shall not constitute an admission that any information cited therein is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b). In the interest of full and complete disclosure to the Office, some or all of the art cited herein may not be considered by Applicant(s) or the Undersigned to be material under the new standards of materiality defined in 37 C.F.R. 1.56(b), enacted March 16, 1992, but may be material under the old standard of materiality defined in 37 C.F.R. 1.56(a), last amended on November 28, 1988, or may merely be technical background which may be of interest to the Examiner. In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b)

within three months of the filing date of the application, or before the mailing date of a first office action on the merits. No fee is required.

Date: 12/29/03

Respectfully submitted,

Duke W. Yee
Registration No. 34,285
CARSTENS, YEE & CAHOON, LLP
P.O. Box 802334
Dallas, Texas 75380
(972) 367-2001

Form PTO-1449

LIST OF PRIOR ART CITED BY APPLICANT
(Use several sheets if necessary)

ATTORNEY DOCKET NO.	SERIAL NO.
YOR920030387US1	**Not Assigned**
APPLICANT **Rhee et al.**	
FILING DATE **October 29, 2003**	GROUP ART UNIT **Not Assigned**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.		PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.		PUBLICATION DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES	NO

OTHER PRIOR ART (*including author, title, date, pertinent page, etc.*)

	AA	**Sidiropoulos et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1683-1692.**

RELATED PATENT APPLICATIONS

EXAMINER INITIAL		APPLICATION NO./ ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE

DATE CONSIDERED	**EXAMINER**

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.